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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/931,104 | 08/17/2001 | Eiji Yoshida | 212881US2 | 3616 |

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/931,104 | YOSHIDA, EIJI | |
| | Examiner | Art Unit | |
| | Johannes P Mondt | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08/20/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *4,6,8,10-12,15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) *4,8,10,12,15 and 17-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Response filed August 20, 2004, forms the basis of this official action. Comments on "Remarks/Arguments" in said Amendment are included below under "Response to Arguments". Claims 6 and 11 remain as the elected claims in the application.

### *Response to Arguments*

1. Applicant's arguments, see "Remarks/Arguments", in the Response filed 8/20/04, with respect to the rejection of claim 6 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made as both claims 6 and 11 were found unpatentable over Mazin et al (USPAT 4,484,088) in view of Paniccia et al (IEEE, Int. Test Conf., as made of record in Information Disclosure Statement of March 18, 2003).

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 6 and 11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazin et al (USPAT 4,484,088) in view of Paniccia et al (Int. Test Conference, IEEE 1998, pp. 740-747 (first made of record through item AW in Information Disclosure Statement filed 3/18/03).

*Mazin et al teach* a semiconductor device (title, abstract and col. 1, l. 5-10), comprising:

a) a second MOS transistor P22 (col. 5, l. 30-36, col. 8, l. 58 and col. 9, l. 2-4: note that the selection silicon dioxide implies P22 is a MOS transistor), including a portion 38 that can be measured by fluctuation in potential, namely gate electrode 38 (col. 5, l. 33-35), said gate electrode 38 being a portion of said MOS transistor P22 with 26/30 as source/drain regions within N- substrate 100, said portion being measurable through the connection by electrical wire as discussed under b) just below;

b) a wire (the wire connecting said gate electrode 38 with diffusion regions 28 and 50) having a first end (right hand side in Figure 3) and a second end (left hand side in Figure 3), the second end being connected with said portion 38 that is measurable (cf. Figure 3); and

c) an observation part, namely: (c1) diffusion region 50 contacted by said wire and (c2) NMOS transistor N46 with gate 62, said observation part including a pn junction (two pn junctions are included therein, namely: one pn junction between P+ diffusion region 28 (col. 5, l. 25-27) and N-type substrate 100 (col. 8, l. 35-42) ), and another pn junction between N+ diffusion region 50 (col. 5, l. 47-51) and P-well 104 (col. 8, l. 49-57) while both pn junctions can be irradiated with a laser beam to detect said fluctuation in potential, because both pn junctions are accessible to monochromatic

radiation while said fluctuation in potential exists (Franz-Keldysh effect) in the event of an electric field across said pn junction; wherein:

1) said observation part includes a (cf. ad (c2) above) a first NMOS transistor N46 (col. 5, l. 55-57), said first MOS transistor including:

(i) a source/drain region 50/54/104/112 (col. 5, l. 44-54 and col. 8, l. 49-57) including a first impurity region 50 of a first conductivity type (N+) (col. 5, l. 47-51), that is connected with said first end of said wire and that is formed within a second impurity region 104 of a second conductivity type (P-type well 104; col. 8, l. 49-57); and a

(ii) a gate electrode 62 (col. 5, l. 55-57) that is electrically insulated from a gate electrode 38 of said second MOS transistor (see Figure 1 wherein: nodes "Q-bar" ( = the symbol 'Q' with a bar over it), to which gate electrode 38 is connected (cf. Fig. 3)) and S, to which gate electrode 62 is connected (cf. Fig. 3) are electrically insulated because Q-bar and S are the second input node and the second normally complementary output nodes, respectively (cf. col. 5, l. 4-8), while input and output nodes are electrically insulated in any working device as otherwise the device cannot perform any function on the input);

2) said pn junction includes said first and second impurity regions 50 and 104 respectively (cf. Figure 3 and see above ad (i)); and

3) said portion that can be measured is said gate electrode 38 of said second MOS transistor (see above).

*Mazin et al do not necessarily teach* (A) said portion that *can be* measured (as discussed above) is *actually being* measured nor (B) said observation part including the

pn junction that *can be* irradiated (as discussed above) is *actually being* irradiated with a laser beam for said detection of said fluctuation in potential.

*However, it would have been obvious* to include, in the semiconductor device, a laser beam irradiating said pn junction *in view of Paniccia et al*, who, in a paper on optical probing by laser light irradiating a silicon substrate teach the testing of the existence of an electric field through laser irradiation of a pn junction as a method of testing MOSFET integrity (see abstract, "Principles of Operation" and "Electroabsorption in P-N junction", particularly Figure 8). Any pn junction can be irradiated in this fashion to determine the electric field condition near the interface between the p-type and n-type domains of the pn junction. Furthermore, straightforward application of the teaching by Paniccia et al in this regard leads to the actual testing of said portion, i.e., said gate electrode 38 for potentials selected on said gate electrode 38 with respect to ground 12 (which is the potential of the P-well 104; see Figure 3) (col. 5, l. 7-9) that are in the range between the ground potential and $V_{DD}$, the latter being the substrate potential, as is ensured by connection through 108 and 106 (see Figure 3) as either the pn junction 28/100 or the pn junction 50/104 is reverse biased in said range.

*Motivation* to include the teaching by Paniccia et al in the invention by Mazin et al derives from the obvious advantage of maximizing the information that can be obtained in the presence of a LVP set-up.

*On claim 11: Mazin et al teach* a semiconductor device (title, abstract and col. 1, l. 5-10), comprising:

a) a second MOS transistor P22 (col. 5, l. 30-36, col. 8, l. 58 and col. 9, l. 2-4: note that the selection silicon dioxide implies P22 is a MOS transistor), including a portion 38 that *can be* measured by fluctuation in potential, namely gate electrode 38 (col. 5, l. 33-35), said gate electrode 38 being a portion of said MOS transistor P22 with 26/30 as source/drain regions within N- substrate 100, said portion being measurable through the connection by electrical wire as discussed under b) just below;

b) a wire (the wire connecting said gate electrode 38 with diffusion regions 28 and 50) having a first end (right hand side in Figure 3) and a second end (left hand side in Figure 3), the second end being connected with said portion 38 that is measurable (cf. Figure 3); and

c) an observation part, including (c1) impurity region 50 contacted by said first end of said wire, (c2) NMOS transistor N46 with gate 62, and (c3) impurity region 28 connected to said wire; said observation part including a pn junction (three pn junctions are included therein, namely: one, henceforth called "second", pn junction between P+ diffusion region 28 (col. 5, l. 25-27) and N-type substrate 100 (col. 8, l. 35-42) ), an additional one called, henceforth called "third", pn junction between a P+ type impurity region 112 and P-well 104 (col. 8, l. 49-57), and another, "first", pn junction between N+ diffusion region 50 (col. 5, l. 47-51) and P-well 104 (col. 8, l. 49-57) while all three pn junctions *can be* irradiated with a laser beam to detect said fluctuation in potential, because all three pn junctions are accessible to monochromatic radiation while said fluctuation in potential exists (Franz-Keldysh effect) in the event of an electric field across any of said pn junctions; wherein:

1) said observation part includes a (cf. ad (c2) above) a first NMOS transistor N46 (col. 5, l. 55-57), said first MOS transistor including:

(i) a source/drain region 50/54/104/112 (col. 5, l. 44-54 and col. 8, l. 49-57) including a first impurity region 50 of a first conductivity type (N+) (col. 5, l. 47-51), that is connected with said first end of said wire and that is formed within a second impurity region 104 of a second conductivity type (P-type well 104; col. 8, l. 49-57); and a

(ii) a gate electrode 62 (col. 5, l. 55-57) that is electrically insulated from a gate electrode 38 of said second MOS transistor (see Figure 1 wherein: nodes "Q-bar" ( = the symbol 'Q' with a bar over it), to which gate electrode 38 is connected (cf. Fig. 3)) and S, to which gate electrode 62 is connected (cf. Fig. 3) are electrically insulated because Q-bar and S are the second input node and the second normally complementary output nodes, respectively (cf. col. 5, l. 4-8), while input and output nodes are electrically insulated in any working device as otherwise the device cannot perform any function on the input);

2) said first pn junction includes said first and second impurity regions 50 and 104 respectively (cf. Figure 3 and see above ad (i)); and

3) said first conductivity type is n-type (N+ is the conductivity type of diffusion region 50: col. 5, l. 47-51, see also above) and said second conductivity type is a p type (p-type conductivity of P-well 104: col. 8, l. 49-57);

4) said observation part further includes:

a second pn junction 28/100 (already called "second" overleaf) (cf. references above and Figure 3) having a third impurity region 28 connected to

said wire (said wire being the wire connecting gate 38 as well as both diffusion regions 28 and 50 through respective metallization areas such as 128 to node Q-bar (cf. Figure 3)) and a fourth impurity region 100 (cf. col. 8, l. 43-47); and

a first fixed potential is applied to said second impurity region 104 through a direct electrical connection with ground potential 12 (col. 5, l. 7-9) and a second fixed potential higher than the first fixed potential is applied to said fourth impurity region 100, namely $V_{DD} > 0$ (namely +), zero being by definition the potential of a ground node including ground node 12.

*Mazin et al do not necessarily teach* (A) said portion that can be measured (as discussed above) is *actually being* measured nor (B) said observation part including the pn junction that can be irradiated by a laser beam (as discussed above) is *actually being* irradiated with a laser beam for said detection of said fluctuation in potential.

*However, it would have been obvious* to include, in the semiconductor device, a laser beam irradiating said pn junction *in view of Paniccia et al*, who, in a paper on optical probing by laser light irradiating a silicon substrate teach the testing of the existence of an electric field through laser irradiation of a pn junction as a method of testing MOSFET integrity (see abstract, "Principles of Operation" and "Electroabsorption in P-N junction", particularly Figure 8). Any pn junction can be irradiated in this fashion to determine the electric field condition near the interface between the p-type and n-type domains of the pn junction. Furthermore, straightforward application of the teaching by Paniccia et al in this regard leads to the actual testing of said portion, i.e., said gate electrode 38 for potentials selected on said gate electrode 38 with respect to ground 12

(which is the potential of the P-well 104; see Figure 3) (col. 5, l. 7-9) that are in the range between the ground potential and $V_{DD}$, the latter being the substrate potential, as is ensured by connection through 108 and 106 (see Figure 3) as either the pn junction 28/100 or the pn junction 50/104 is reverse biased in said range.

*Motivation* to include the teaching by Paniccia et al in the invention by Mazin et al derives from the obvious advantage of maximizing the information that can be obtained in the presence of a LVP set-up.

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
October 13, 2004

Patent Examiner:

Johannes Mondt (Art Unit: 2826)